Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for forming a semiconductor structure in manufacturing a semiconductor device, comprising:

providing a pad layer on a surface of a substrate;

providing a nitride layer on the pad layer;

providing a sacrificial oxide layer on the nitride layer;

in a first etching step, etching at least the sacrificial oxide and nitride layers to define opposing substantially vertical surfaces of at least the sacrificial oxide and nitride layers;

in a second etching step, etching the nitride layer such that the opposing substantially vertical surfaces of the nitride layer are recessed from the opposing substantially vertical surfaces of the sacrificial oxide layer, the sacrificial oxide layer substantially preventing the nitride layer from decreasing in thickness as a result of the etching of the nitride layer; and

in a third etching step, etching the substrate to form a trench extending into the substrate for purposes of defining one or more isolation regions adjacent the trench;

wherein the first etching step comprises etching the pad layer, in addition to etching sacrificial oxide and nitride layers, to define opposing substantially vertical surfaces of the pad layer; and

wherein the first etching step comprises etching a portion of the substrate, in addition to etching the sacrificial oxide, nitride, and pad layers, to define opposing substantially vertical surfaces of the substrate.

2. (Original) The method of Claim 1, wherein nitride layer comprises at least one of:

silicon nitride;

silicon-rich silicon nitride; and

silicon oxy-nitride.

3. (Cancelled)

4. (Cancelled)

5. (Currently Amended) The method of Claim [4]1, wherein the opposing substantially vertical portions of the substrate have a height of approximately 100Å to approximately 200Å.

6. (Currently Amended) ~~The method of Claim 1,~~ A method for forming a semiconductor structure in manufacturing a semiconductor device, comprising:

providing a pad layer on a surface of a substrate;

providing a nitride layer on the pad layer;

providing a sacrificial oxide layer on the nitride layer;

in a first etching step, etching at least the sacrificial oxide and nitride layers to define opposing substantially vertical surfaces of at least the sacrificial oxide and nitride layers;

in a second etching step, etching the nitride layer such that the opposing substantially vertical surfaces of the nitride layer are recessed from the opposing substantially vertical surfaces of the sacrificial oxide layer, the sacrificial oxide layer substantially preventing the nitride layer from decreasing in thickness as a result of the etching of the nitride layer; and

in a third etching step, etching the substrate to form a trench extending into the substrate for purposes of defining one or more isolation regions adjacent the trench; and

further comprising, subsequent to the second etching step and prior to the third etching step:

etching the pad layer to define opposing substantially vertical surfaces of the pad layer; and

etching a portion of the substrate to define opposing substantially vertical surfaces of the substrate.

7. (Original) The method of Claim 1, wherein the second etching step comprises wet etching the nitride layer using a phosphoric acid.

8. (Original) The method of Claim 1, wherein the second etching step comprises dry etching the nitride layer using a plasma etcher.

9. (Original) The method of Claim 8, wherein the entire method is performed in the plasma etcher without removing the semiconductor structure from the plasma etcher.

10. (Currently Amended) A semiconductor structure used in manufacturing a semiconductor device, comprising:

a pad layer provided on a surface of a substrate;

a nitride layer provided on the pad layer; and

a sacrificial oxide layer provided on the nitride layer;

at least the sacrificial oxide and nitride layers having been etched in a first etching step to define opposing substantially vertical surfaces of at least the sacrificial oxide and nitride layers;

the nitride layer having been etched in a second etching step such that the opposing substantially vertical surfaces of the nitride layer are recessed from the opposing substantially vertical surfaces of the sacrificial oxide layer, the sacrificial oxide layer substantially preventing the nitride layer from decreasing in thickness as a result of the etching of the nitride layer; and

the substrate having been etched in a third etching step to form a trench extending into the substrate for purposes of defining one or more isolation regions adjacent the trench;

wherein, subsequent to the second etching step and prior to the third etching step:

the pad layer was etched to define opposing substantially vertical surfaces of the pad layer; and

a portion of the substrate was etched to define opposing substantially vertical surfaces of the substrate.

11. (Original) The semiconductor structure of Claim 10, wherein nitride layer comprises at least one of:

silicon nitride;

silicon-rich silicon nitride; and

silicon oxy-nitride.

12. (Original) The semiconductor structure of Claim 10, wherein the pad layer was etched in the first etching step, in addition to etching sacrificial oxide and nitride layers, to define opposing substantially vertical surfaces of the pad layer.

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Original) The semiconductor structure of Claim 10, wherein the second etching step comprises wet etching the nitride layer using a phosphoric acid.

17. (Original) The semiconductor structure of Claim 10, wherein the second etching step comprises dry etching the nitride layer using a plasma etcher.

18. (Original) The semiconductor structure of Claim 17, wherein the first, second, and third etching steps for forming the semiconductor structure were performed

in the plasma etcher without removing the semiconductor structure from the plasma etcher.

19. (Cancelled)

20. (Cancelled)